Low-Noise Matched Dual PNP Transistor

MAT03

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/aerospace is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/MAT03

2.0 Part Number. The complete part number(s) of this specification follow:

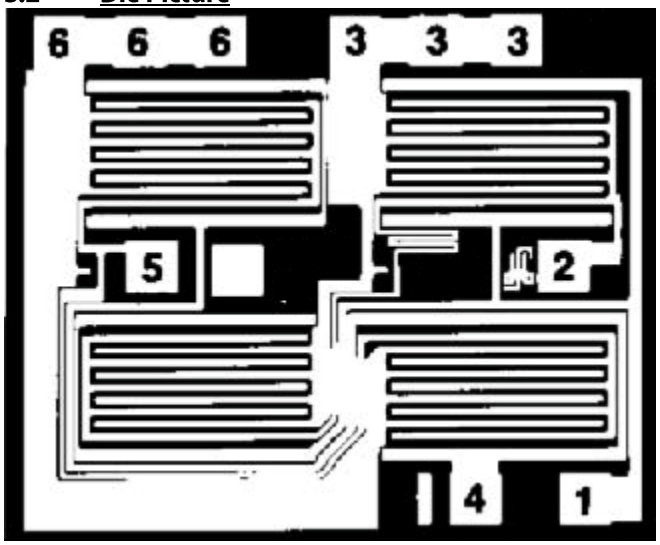
Part Number	Description
MAT03-000C	Low-Noise Matched Dual PNP Transistor

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
70 mil x 60 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



Substrate can be connected to V- or floated.

1. C1
2. B1
3. E1
4. C2
5. B2
6. E2

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3.3 Absolute Maximum Ratings 1/

Collector to Base Voltage (BV_{CBO}) 36V
Collector to Emitter Voltage (BV_{CEO}) 36V
Collector to Collector Voltage (BV_{CC}) 36V
Emitter to Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Junction Temperature (T_J)..... .....+150°C
Ambient Operating Temperature Range..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Absolute Maximum Ratings Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Sample Size and Qual Acceptance Criteria – 25/2

(b) Qual Sample Package – 6 Lead Can Package (TO)

(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Current Gain	h_{FE}	I_C=1mA; V_{CB} = 0V, -36V	100		
		I_C=100µA,V_{CB}=0V,-36V	90		
		I_C=10µA; V_{CB} = 0V,-36V	80		
Current Gain Match 2/	$•h_{FE}$	I_C = 100µA; V_{CB} = 0V		3	%
Offset Voltage	V_{OS}	V_{CB} = 0V		100	µV
Offset Voltage Change vs. V_{CB}	$•V_{OS}$ /$•V_{CB}$	V_{CB} = 0V, -36V		150	µV
Offset Voltage Change vs. Collector Current	$•V_{OS}/•I_C$	I_C1 = 10µA, I_C2 = 1mA, V_{CB} = 0V		50	µV
Input Offset Current	I_{OS}	V_{CB} = 0V, I_C = 100µA		35	nA
Bulk Emitter Resistance	r_{BE}			0.75	Ω
Collector Base Leakage Current	I_{CBO}	V_{CB} = -36V		200	pA
Collector Saturation Voltage	$V_{CE}SAT$	I_C = 1mA, I_B=100µA		0.1	V

Table I Notes:

1/ V_{CB} = -15V, I_C = 10µA, T_A = 25°C, unless otherwise specified.

2/ Current gain match (□h_{FE}) is defined as: □h_{FE} = $\frac{100(\Delta I_B)h_{FE}\min}{I_C}$.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Current Gain	h_{FE}	I_C=1mA; V_{CB} = 0V,-36V	1	90		
			2, 3	60		
		I_C=100µA,V_{CB} =0V,-36V	1	80		
		I_C=100µA, V_{CB} =-36V	2, 3	50		
		I_C=10µA; V_{CB} = 0V,-36V	1	70		
		I_C=10µA; V_{CB} = -36V	2, 3	40		
Current Gain Match 2/	Δh_{FE}	I_C = 100µA; V_{CB} = 0V	1		3	%
Offset Voltage	V_{OS}	V_{CB} = 0V	1		120	µV
			2, 3		180	
Change in Offset Voltage vs. Temperature 3/	TCV_{OS}	V_{CB} = 0V			0.5	µV/°C
Offset Voltage Change vs. V_{CB}	$\bullet V_{OS}/\bullet V_{CB}$	V_{CB} = 0V, -36V	1		170	µV
Offset Voltage Change vs. Collector Current	$\bullet V_{OS}/\bullet I_C$	I_C1 = 10µA, I_C2 = 1mA, V_{CB} =0V	1		70	µV
Input Offset Current	I_{OS}	V_{CB} = 0V, I_C = 100µA	1		55	nA
Bulk Emitter Resistance	r_{BE}		1		0.9	Ω
Collector Base Leakage Current	I_{CBO}	V_{CB} = -36V	1		250	pA
Collector Saturation Voltage	$V_{CE}SAT$	I_C = 1mA, I_B = 100µA	1		0.1	V
Breakdown Voltage	BV_{CEO}		1	36		V

Table II Notes:

1/ V_{CB} = -15V, I_C = 10µA, unless otherwise specified.

2/ Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FE}\min}{I_C}$.

3/ Guaranteed by V_{OS} test $\left(TCV_{OS} \cong \frac{V_{OS}}{T} \text{ for } V_{OS} << V_{BE} \right)$ T = 298 °K for T_A = +25°C.

Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table II with the following exceptions)								
Parameter	**Symbol**	**Sub-groups**	**Post Burn In Limit**		**Post Life Test Limit**		**Life Test Delta**	**Units**
			Min	**Max**	**Min**	**Max**		
Current Gain @ 1mA	h_{FE}	1	90		80		±40	
		2, 3			50			
Current Gain @ 100••	h_{FE}	1	80		70		±36	
		2, 3			40			
Current Gain @ 10••	h_{FE}	1	70		60		±32	
		2, 3			30			
Input Offset Current	I_{OS}	1		55		75	±20	nA
		2, 3						

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition A, B, or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Feb. 28, 2002
B	Update web address. Change ΔhFE condition on table II from 10uA to 100uA.	Aug. 11, 2003
C	Edit pqalib ecn rev history to add "Change ΔhFE condition on table II from 10uA to 100uA."	Oct. 20, 2003
D	Update header/footer and add to 1.0 Scope description.	Feb. 29,2008
E	Add Junction Temperature & Ambient Operating Temperature Range to section 3.3-Absolute Maximum Ratings.	April 3, 2008
F	Updated Section 4.0c note to indicated pre-screen temp testing being performed.	June 5 2009
G	Updated fonts and sizes to ADI standards	Oct. 7, 2011